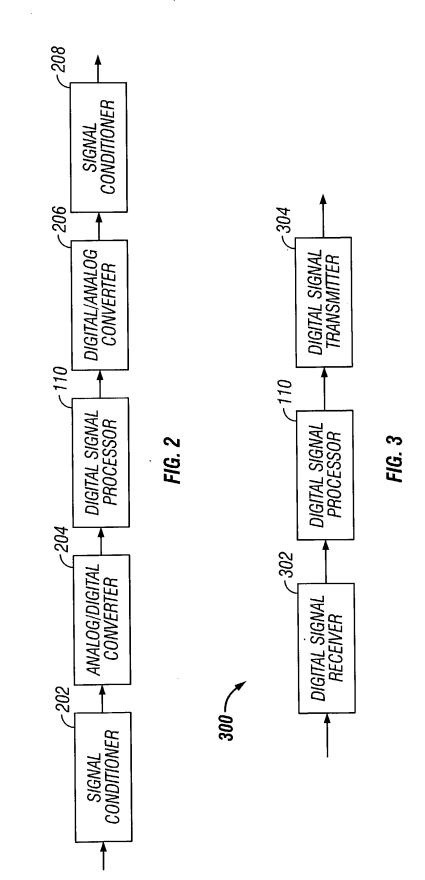


FIG. 1

2/**4**



DIGITAL SIGNAL PROCESSOR WITH MULTIPLE INSTRUCTION DESTINATIONS FOR A PIPELINED SYSTEM

Gregory A. Overkamp et al.

09/675,816

10559-270001

	<u></u>								
	IF1	IF2	DEC	AC	EX1	EX2	EX3	WB	
1	i								
2	i+1	i							
3	i+2	i+1	i						
•••	•••	i+2	i+1	•••					
•••	•••	•••	i+2	•••	•••				
n	i+(n-1)	•••	•••	•••	•••	•••			

- CLOCK CYCLE

FIG. 4

10559-270001



4/4

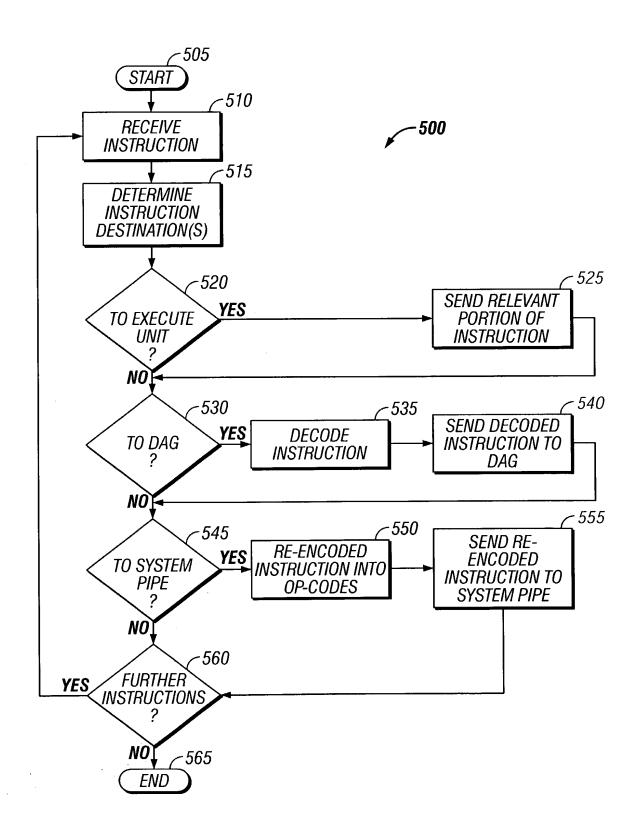


FIG. 5